



G31T-M9 V : 7.0

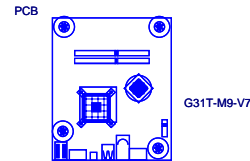
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REVISION HISTORY:

Rev	Date	Notes
A	2008.10.22	1. DEL PCI2/FDD/IR/SPDIF/CD_IN 2. LPT/COM change to Header 3. Del 2*SATA/1*F_USB/SYS_FAN 4. Del IP1 5. del vcore 2*output cap retain
1.0	2009.01.09	1. change vcore ocp setting/current balance 2. VGA part layout for noise 3. Vcore layout for thermal 4. KBMPWR for PS2 only 5. PWM vin cap change to os-con 6. Vcore output cap change 4*os-con
7.0	2009.09.10	1. change LAN to RTL8111DL/8103EL for EUP



Notes:

- 1). "PWR" net means inner power plane under impedance trace.
- 2). "GND" net means inner ground plane under impedance trace.
- 3). IP1 footprint is J2X2_IP
- 4). After netlist running, please specially take care the single net name: "IMPEDANCE_T" and "IMPEDANCE_B".

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.



3) DESIGN NOTES in red are critical, and must be understood and followed.



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Title			
Cover Page			
Size	Document Number		Rev
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DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1

VCORE POWER
PWM VRD11
(RT8802A)

INTEL
P4 Processor
Core 2 Duo & Wolfdale
LGA 775 pin

CLOCK GEN:9LPRS437

FSB : 1066MHz & Freq : 266MHz
FSB : 800MHz & Freq : 200MHz

BW : 10.7GB/s @ DDR2 :800/667MHz

PCIEx16

INTEL
G31
1210pin FC-BGA

DIMM1: DDR2 Socket 240P

DIMM2 : DDR2 Socket 240P

VGA

Analog Display
RAMDAC: 400MHz
Resolutions Up To 2048x1536@75Hz

BW : 2GB/s

USB V2.0

USB1
2 ports

USB2
2 ports

USB3
2 ports

Up to Ultra ATA/100

IDE1 40pin

One IDE Channel

INTEL
ICH7
652pin EPGA

PCIEx1
BW : 133MB/s @Freq : 33MHz

PCI1 Slot 120pin @ AD17
PCI2 Slot 120pin @ AD18

PCIE-LAN
PCIE LAN L1e/L2-48

USBLAN
RJ45

Line in
Line out
Mic in

Audio Codec
VT1708B

Azalia I/F


Flash Bios

Super I/O
IT8713F
128pin PQFP

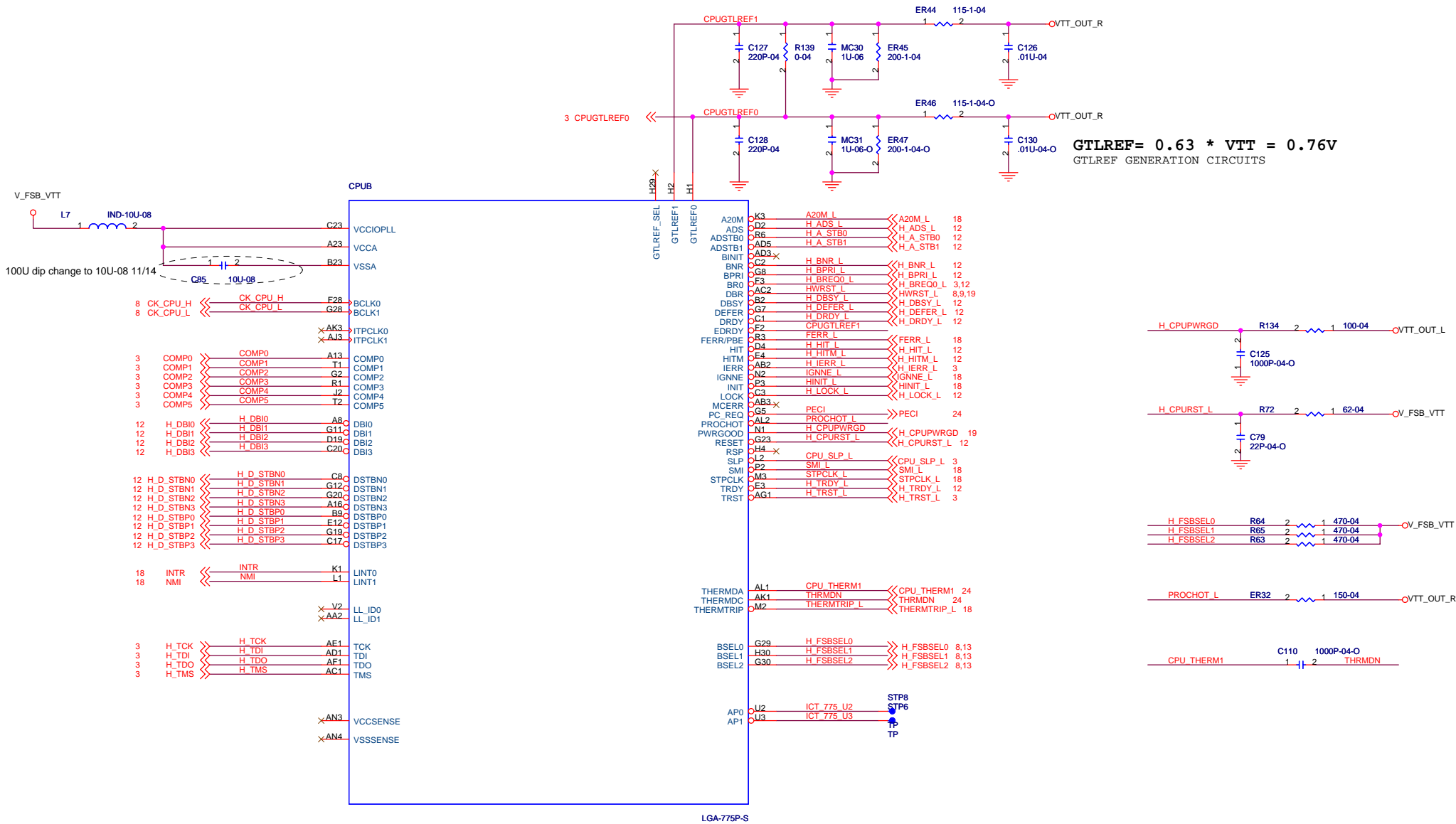
LPC bus

SATA1 7Pin
SATA2 7pin
SATA3 7Pin
SATA4 7pin

BW : 150MB/s

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Title System Block Diagram		
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VCCP

VCCP

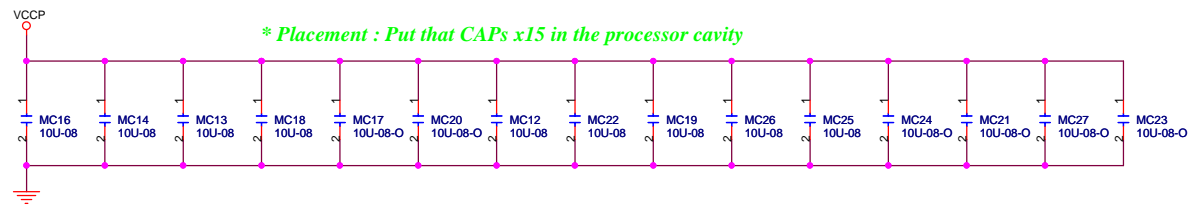
CPUC
LGA-775P-S

AM8	VCC122
AM9	VCC123
AN10	VCC124
AN11	VCC125
AN14	VCC126
AN15	VCC127
AN18	VCC128
AN19	VCC129
AN20	VCC130
AN21	VCC131
AN25	VCC132
AN26	VCC133
AN29	VCC134
AN30	VCC135
AN31	VCC136
AN32	VCC137
J10	VCC138
J11	VCC139
J12	VCC140
J13	VCC141
J14	VCC142
J15	VCC143
J18	VCC144
J19	VCC145
J20	VCC146
J21	VCC147
J22	VCC148
J23	VCC149
J24	VCC150
J25	VCC151
J26	VCC152
J27	VCC153
J28	VCC154
J29	VCC155
J30	VCC156
J31	VCC157
J8	VCC158
K23	VCC159
K24	VCC160
K25	VCC161
K26	VCC162
K27	VCC163
K28	VCC164
K29	VCC165
K30	VCC166
K8	VCC167
L8	VCC168
M24	VCC169
M25	VCC170
M26	VCC171
M27	VCC172
M28	VCC173
M29	VCC174
M30	VCC175
M31	VCC176
M8	VCC177
N23	VCC178
N24	VCC179
N25	VCC180
N26	VCC181
N27	VCC182
N28	VCC183
N29	VCC184
N30	VCC185
N8	VCC186
P8	VCC187
R8	VCC188
T23	VCC189
T24	VCC190
T25	VCC191
T26	VCC192
T27	VCC193
T28	VCC194
T29	VCC195
T8	VCC196
U23	VCC197
U24	VCC198
U25	VCC199
U26	VCC200
U28	VCC201
U29	VCC202
U30	VCC203
U31	VCC204
U8	VCC205
U8	VCC206
W23	VCC207
W24	VCC208
W25	VCC209
W26	VCC210
W27	VCC211
W28	VCC212
W29	VCC213
W30	VCC214
W8	VCC215
Y23	VCC216
Y24	VCC217
Y25	VCC218
Y26	VCC219
Y27	VCC220
Y28	VCC221
Y29	VCC222
Y8	VCC223
Y8	VCC224
	VCC225

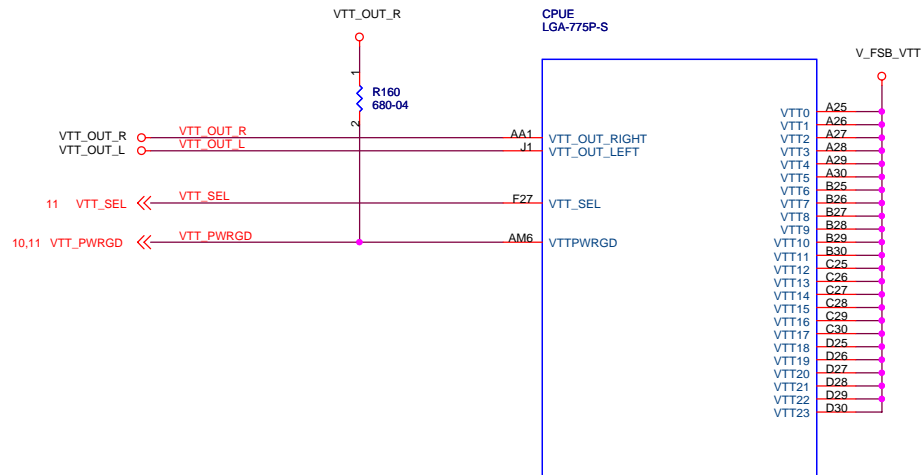
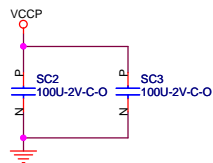
AA8	VCC0
AB8	VCC1
AC23	VCC2
AC24	VCC3
AC25	VCC4
AC26	VCC5
AC27	VCC6
AC28	VCC7
AC29	VCC8
AC30	VCC9
AC8	VCC10
AD23	VCC11
AD24	VCC12
AD25	VCC13
AD26	VCC14
AD27	VCC15
AD28	VCC16
AD29	VCC17
AD30	VCC18
AE11	VCC19
AE12	VCC20
AE14	VCC21
AE15	VCC22
AE16	VCC23
AE17	VCC24
AE19	VCC25
AE21	VCC26
AE22	VCC27
AE23	VCC28
AE24	VCC29
AE25	VCC30
AF12	VCC31
AF14	VCC32
AF15	VCC33
AF16	VCC34
AF18	VCC35
AF19	VCC36
AF21	VCC37
AF22	VCC38
AF8	VCC39
AG11	VCC40
AG12	VCC41
AG14	VCC42
AG15	VCC43
AG18	VCC44
AG19	VCC45
AG21	VCC46
AG22	VCC47
AG25	VCC48
AG28	VCC49
AG29	VCC50
AG30	VCC51
AG8	VCC52
AG9	VCC53
AH11	VCC54
AH12	VCC55
AH14	VCC56
AH15	VCC57
AH18	VCC58
AH19	VCC59
AH21	VCC60
AH22	VCC61
AH23	VCC62
AH25	VCC63
AH26	VCC64
AH27	VCC65
AH28	VCC66
AH29	VCC67
AH30	VCC68
AH8	VCC69
AH9	VCC70
AI11	VCC71
AI12	VCC72
AI14	VCC73
AI15	VCC74
AI18	VCC75
AI19	VCC76
AI21	VCC77
AI22	VCC78
AI25	VCC79
AI26	VCC80
AI8	VCC81
AI9	VCC82
AK11	VCC83
AK12	VCC84
AK14	VCC85
AK15	VCC86
AK18	VCC87
AK19	VCC88
AK21	VCC89
AK22	VCC90
AK25	VCC91
AK26	VCC92
AK8	VCC93
AL11	VCC94
AL12	VCC95
AL14	VCC96
AL15	VCC97
AL18	VCC98
AL19	VCC99
AL21	VCC100
AL22	VCC101
AL25	VCC102
AL26	VCC103
AL28	VCC104
AL30	VCC105
AL8	VCC106
AL9	VCC107
AM11	VCC108
AM12	VCC109
AM14	VCC110
AM15	VCC111
AM18	VCC112
AM19	VCC113
AM21	VCC114
AM22	VCC115
AM25	VCC116
AM26	VCC117
AM28	VCC118
AM29	VCC119
AM23	VCC120
AM30	VCC121

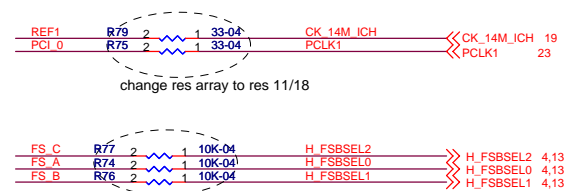
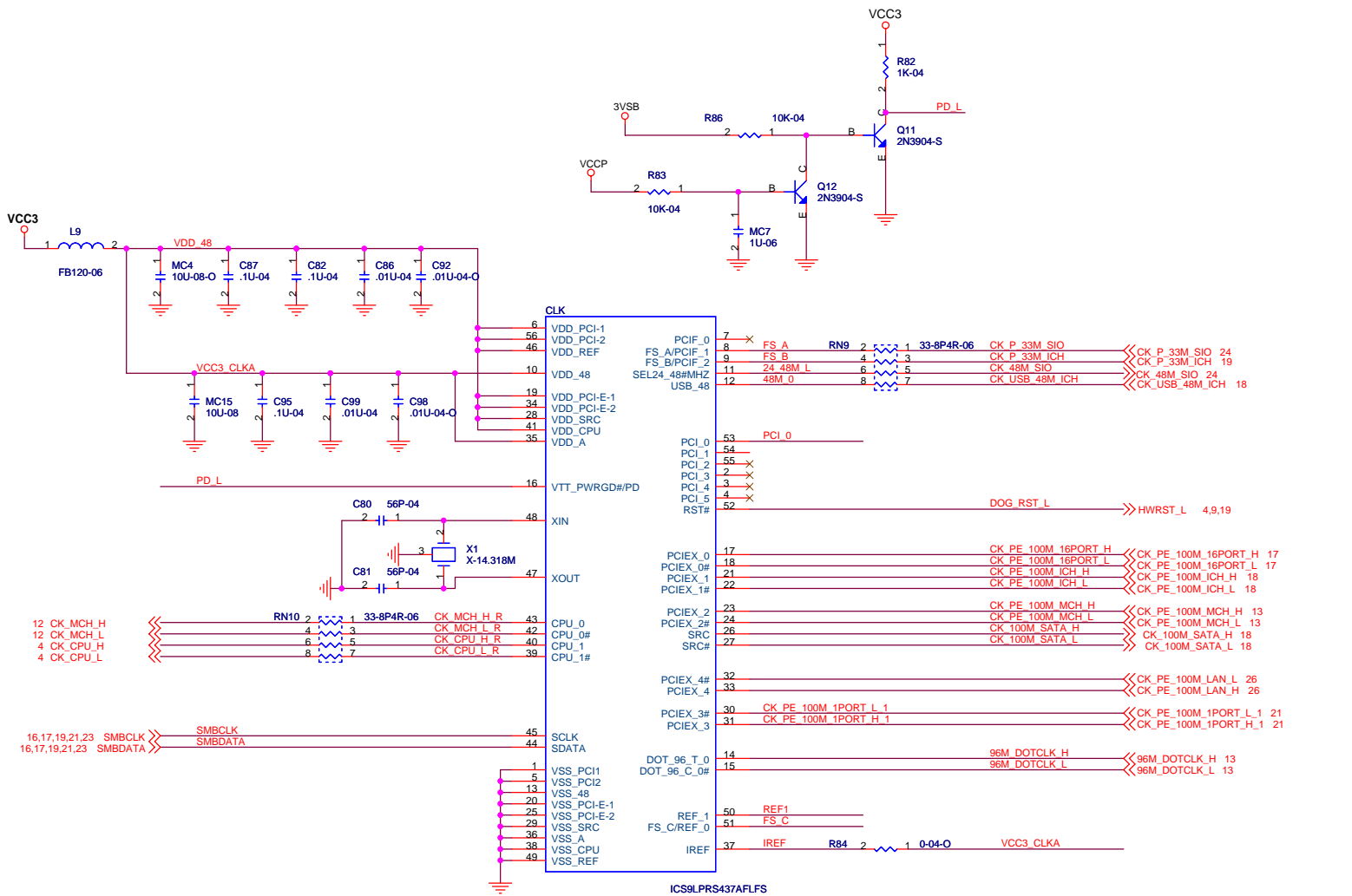
**Elitegroup Computer Systems**

Title P4 LGA775P Part C		
Size Custom	Document Number G31T-M9	Rev 7.0
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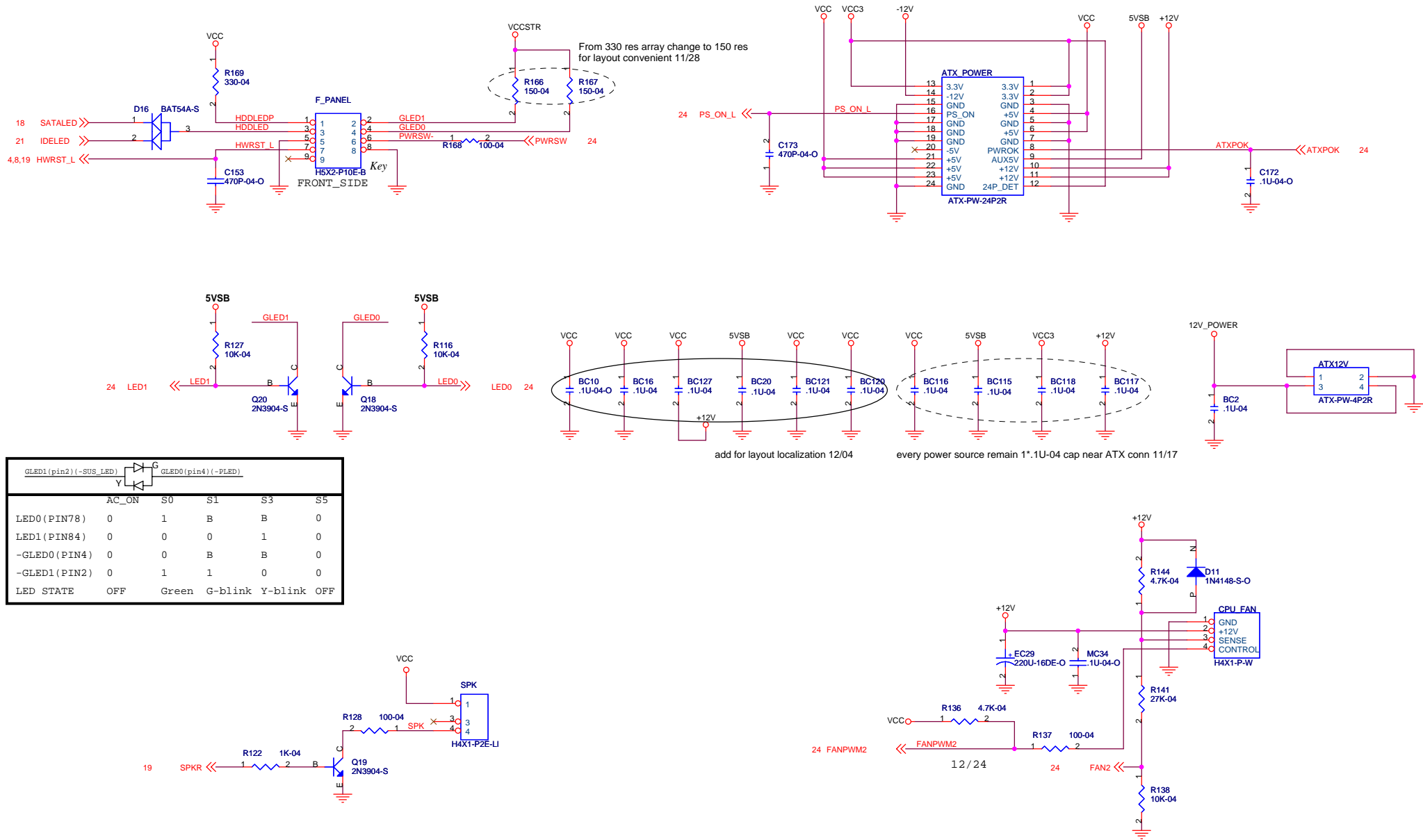


* Placement : Put that CAPs x2 on solder side

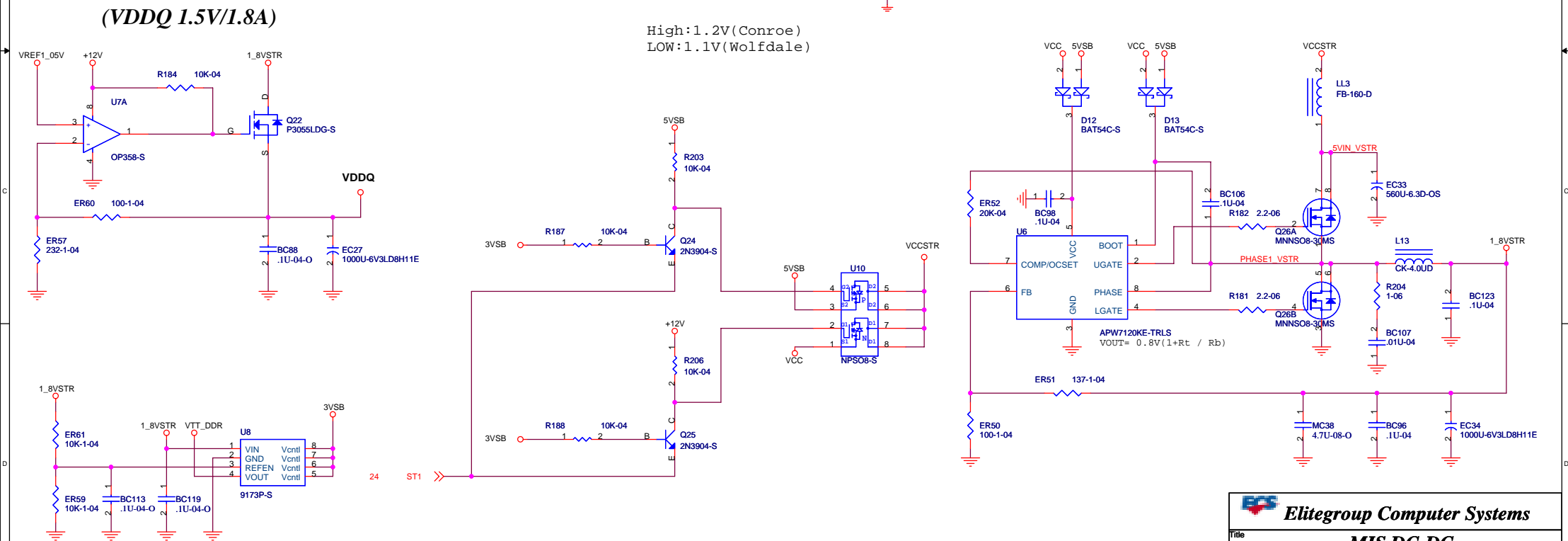




Swap PCIEX16 and SATA clock
Change ICH clk to pin 8

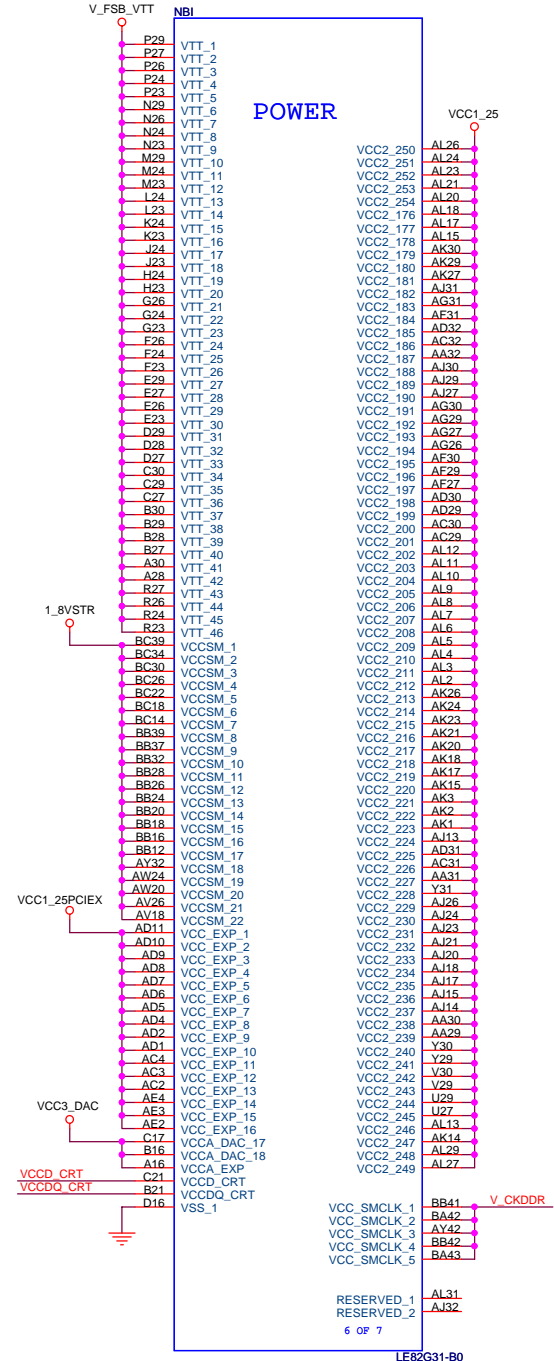
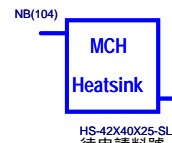
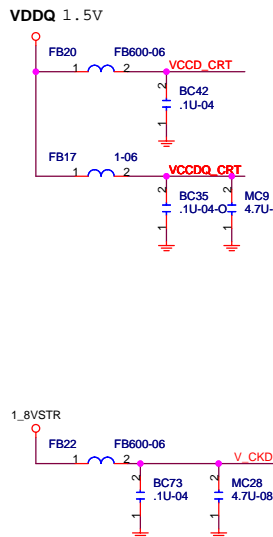
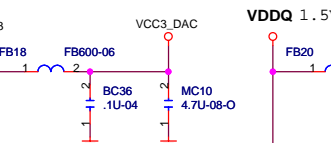
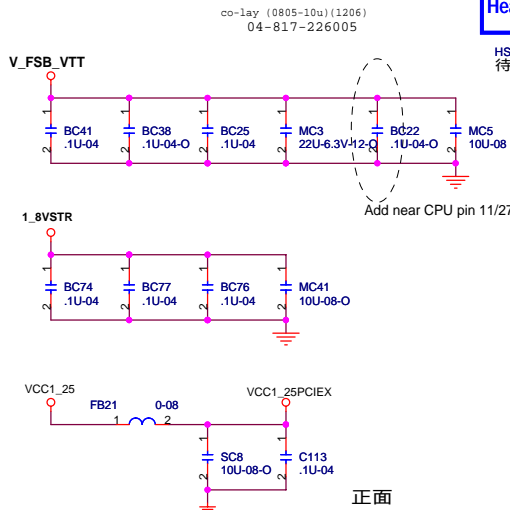
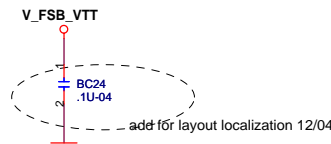
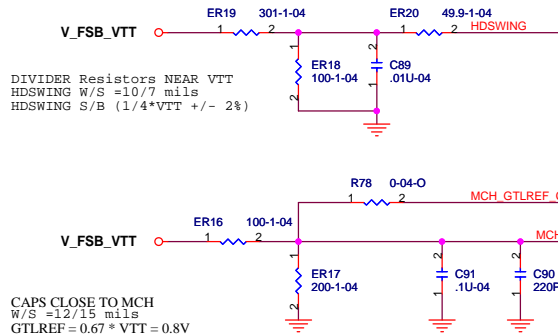
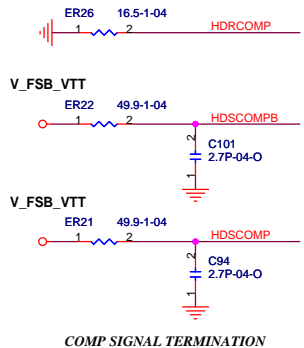


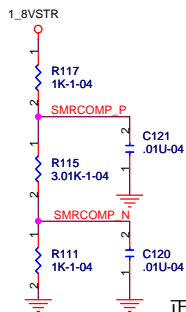
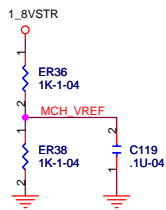
	AC_ON	S0	S1	S3	S5
LED0 (PIN78)	0	1	B	B	0
LED1 (PIN84)	0	0	0	1	0
-GLED0 (PIN4)	0	0	B	B	0
-GLED1 (PIN2)	0	1	1	0	0
LED STATE	OFF	Green	G-blink	Y-blink	OFF



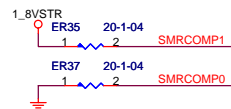
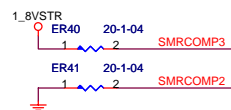
NBB				F5B			
3	H_A3	H_A3	J42	HA3#	HD0#	R40	H_D0
3	H_A4	H_A4	L39	HA4#	HD1#	P41	H_D1
3	H_A5	H_A5	J40	HA5#	HD2#	R41	H_D2
3	H_A6	H_A6	L36	HA6#	HD3#	R42	H_D3
3	H_A7	H_A7	K42	HA7#	HD4#	M39	H_D5
3	H_A8	H_A8	N32	HA8#	HD5#	N41	H_D6
3	H_A9	H_A9	N34	HA9#	HD6#	N42	H_D7
3	H_A10	H_A10	N38	HA10#	HD7#	L41	H_D8
3	H_A11	H_A11	M38	HA11#	HD8#	J39	H_D9
3	H_A12	H_A12	M36	HA12#	HD9#	K42	H_D10
3	H_A13	H_A13	L32	HA13#	HD10#	J41	H_D11
3	H_A14	H_A14	R34	HA14#	HD11#	K41	H_D12
3	H_A15	H_A15	N35	HA15#	HD12#	G40	H_D13
3	H_A16	H_A16	N38	HA16#	HD13#	F41	H_D14
3	H_A17	H_A17	U37	HA17#	HD14#	F42	H_D15
3	H_A18	H_A18	R37	HA18#	HD15#	C42	H_D16
3	H_A19	H_A19	P42	HA19#	HD16#	D41	H_D17
3	H_A20	H_A20	R38	HA20#	HD17#	F38	H_D18
3	H_A21	H_A21	U36	HA21#	HD18#	G37	H_D19
3	H_A22	H_A22	U33	HA22#	HD19#	E42	H_D20
3	H_A23	H_A23	U36	HA23#	HD20#	E39	H_D21
3	H_A24	H_A24	U33	HA24#	HD21#	E37	H_D22
3	H_A25	H_A25	U33	HA25#	HD22#	C39	H_D23
3	H_A26	H_A26	U33	HA26#	HD23#	C39	H_D24
3	H_A27	H_A27	U33	HA27#	HD24#	C33	H_D25
3	H_A28	H_A28	Y34	HA28#	HD25#	A37	H_D26
3	H_A29	H_A29	Y34	HA29#	HD26#	F33	H_D27
3	H_A30	H_A30	V42	HA30#	HD27#	E35	H_D28
3	H_A31	H_A31	V38	HA31#	HD28#	K32	H_D29
3	H_A32	H_A32	V36	HA32#	HD29#	A32	H_D30
3	H_A33	H_A33	V38	HA33#	HD30#	B34	H_D31
3	H_A34	H_A34	V38	HA34#	HD31#	J31	H_D32
3	H_A35	H_A35	AA37	HA35#	HD32#	F32	H_D33
3	H_REQ0	H_REQ0	F40	HREQ0#	HD33#	M31	H_D34
3	H_REQ1	H_REQ1	L38	HREQ1#	HD34#	E31	H_D35
3	H_REQ2	H_REQ2	G43	HREQ2#	HD35#	K31	H_D36
3	H_REQ3	H_REQ3	J37	HREQ3#	HD36#	G29	H_D37
3	H_REQ4	H_REQ4	J37	HREQ4#	HD37#	R27	H_D38
4	H_A_STB0	H_A_STB0	M34	HADSTB0#	HD38#	E31	H_D39
4	H_A_STB1	H_A_STB1	U34	HADSTB1#	HD39#	J29	H_D40
4	H_D_STBP0	H_D_STBP0	L40	HDSTBP0#	HD40#	F28	H_D41
4	H_D_STBN0	H_D_STBN0	M43	HDSTBN0#	HD41#	L27	H_D42
4	H_D_STBP1	H_D_STBP1	M40	HDSTBP1#	HD42#	K27	H_D43
4	H_D_STBN1	H_D_STBN1	C35	HDSTBN1#	HD43#	H26	H_D44
4	H_D_STBP2	H_D_STBP2	J33	HDSTBP2#	HD44#	L26	H_D45
4	H_D_STBN2	H_D_STBN2	H33	HDSTBN2#	HD45#	J26	H_D46
4	H_D_STBP3	H_D_STBP3	G27	HDSTBP3#	HD46#	M28	H_D47
4	H_D_STBN3	H_D_STBN3	H27	HDSTBN3#	HD47#	C33	H_D48
4	H_D_STBP4	H_D_STBP4	C28	HDSTBP4#	HD48#	C35	H_D49
4	H_D_STBN4	H_D_STBN4	D38	HDSTBN4#	HD49#	E41	H_D50
4	H_D_STBP5	H_D_STBP5	B38	HDSTBP5#	HD50#	B41	H_D51
4	H_D_STBN5	H_D_STBN5	E33	HDSTBN5#	HD51#	D42	H_D52
4	H_D_STBP6	H_D_STBP6	D38	HDSTBP6#	HD52#	C40	H_D53
4	H_D_STBN6	H_D_STBN6	E33	HDSTBN6#	HD53#	D35	H_D54
4	H_D_STBP7	H_D_STBP7	E33	HDSTBP7#	HD54#	B40	H_D55
4	H_D_STBN7	H_D_STBN7	E33	HDSTBN7#	HD55#	C38	H_D56
4	H_D_STBP8	H_D_STBP8	E33	HDSTBP8#	HD56#	D37	H_D57
4	H_D_STBN8	H_D_STBN8	E33	HDSTBN8#	HD57#	B33	H_D58
4	H_D_STBP9	H_D_STBP9	E33	HDSTBP9#	HD58#	D33	H_D59
4	H_D_STBN9	H_D_STBN9	E33	HDSTBN9#	HD59#	C34	H_D60
4	H_D_STBP10	H_D_STBP10	E33	HDSTBP10#	HD60#	B35	H_D61
4	H_D_STBN10	H_D_STBN10	E33	HDSTBN10#	HD61#	A32	H_D62
4	H_D_STBP11	H_D_STBP11	E33	HDSTBP11#	HD62#	D32	H_D63
4	H_D_STBN11	H_D_STBN11	E33	HDSTBN11#	HD63#	D32	H_D63

LE82G31-80





DESIGN NOTE:
BUFFERS CALIBRATE TO
20/80% OF V_{SM} INTERNAL
BUFFERS SET TO 20 OHMS



NBC		ULMCH	
MAAA_0	BA31	SMA_A0	SDQS_A0
MAAA_1	BA25	SMA_A1	SDQS_A0#
MAAA_2	BA26	SMA_A2	SDM_A0
MAAA_3	BA25	SMA_A3	
MAAA_4	AY25	SMA_A4	SDQ_A0
MAAA_5	BA23	SMA_A5	SDQ_A1
MAAA_6	AY24	SMA_A6	SDQ_A2
MAAA_7	AY23	SMA_A7	SDQ_A3
MAAA_8	BB23	SMA_A8	SDQ_A4
MAAA_9	BA22	SMA_A9	SDQ_A5
MAAA_10	AY33	SMA_A10	SDQ_A6
MAAA_11	BB22	SMA_A11	SDQ_A7
MAAA_12	AW21	SMA_A12	
MAAA_13	AY38	SMA_A13	SDQS_A1
MAAA_14	BA21	SMA_A14	SDQS_A1#
			SDM_A1
SWE_L_A	BB34	SWE_A#	
SCAS_L_A	AY35	SCAS_A#	SDQ_A8
SRAS_L_A	BB35	SRAS_A#	SDQ_A9
			SDQ_A10
SBSA_0	BA33	SBS_A0	SDQ_A11
SBSA_1	AW32	SBS_A1	SDQ_A12
SBSA_2	BB21	SBS_A2	SDQ_A13
			SDQ_A14
CSA_L0	AW35	SCS_A0#	SDQ_A15
CSA_L1	BA35	SCS_A1#	
	BA34	RESERVED_11	
	BB38	RESERVED_12	SDQS_A2
			SDM_A2
CKEA_0	BC20	SCKE_A0	SDQ_A16
CKEA_1	AY20	SCKE_A1	SDQ_A17
	AY21	RESERVED_9	SDQ_A18
	BA19	RESERVED_10	SDQ_A19
ODTA_0	AY37	SODT_A0	SDQ_A20
ODTA_1	BA38	SODT_A1	SDQ_A21
	BB35	RESERVED_2	SDQ_A22
	BA39	RESERVED_1	SDQ_A23
DCLKA_H0	AU31	SCLK_A0	SDQS_A3
DCLKA_L0	AR31	SCLK_A0#	SDQS_A3#
DCLKA_H1	AP27	SCLK_A1	SDM_A3
DCLKA_L1	AN27	SCLK_A1#	
DCLKA_H2	AV33	SCLK_A2	SDQ_A24
DCLKA_L2	AW33	SCLK_A2#	SDQ_A25
	AP29	RESERVED_3	SDQ_A26
	AP31	RESERVED_4	SDQ_A27
	AM26	RESERVED_5	SDQ_A28
	AM27	RESERVED_6	SDQ_A29
	AT33	RESERVED_7	SDQ_A30
	AU33	RESERVED_8	SDQ_A31
			SDQS_A4
			SDQS_A4#
			SDM_A4
			SDQ_A32
			SDQ_A33
			SDQ_A34
			SDQ_A35
			SDQ_A36
			SDQ_A37
			SDQ_A38
			SDQ_A39
SDQS_A5		AL41	DQS_H_A5
SDQS_A5#		AL40	DQS_L_A5
SDM_A5		AM43	MPD_A5
			SDQ_A40
			SDQ_A41
			SDQ_A42
			SDQ_A43
			SDQ_A44
			SDQ_A45
			SDQ_A46
			SDQ_A47
SDQS_A6		AG42	DQS_H_A6
SDQS_A6#		AG41	DQS_L_A6
SDM_A6		AG40	MPD_A6
			SDQ_A48
			SDQ_A49
			SDQ_A50
			SDQ_A51
			SDQ_A52
			SDQ_A53
			SDQ_A54
			SDQ_A55
SDQS_A7		AC42	DQS_H_A7
SDQS_A7#		AC41	DQS_L_A7
SDM_A7		AC40	MPD_A7
			SDQ_A56
			SDQ_A57
			SDQ_A58
			SDQ_A59
			SDQ_A60
			SDQ_A61
			SDQ_A62
			SDQ_A63

DDR_0

AN21

RESERVED

3 OF 7

LE82G31-B0

NBD		ULMCH	
MAAB_0	BB17	SMA_B0	SDQS_B0
MAAB_1	AY17	SMA_B1	SDQS_B0#
MAAB_2	BA17	SMA_B2	SDM_B0
MAAB_3	BC16	SMA_B3	
MAAB_4	AW15	SMA_B4	SDQ_B0
MAAB_5	BA15	SMA_B5	SDQ_B1
MAAB_6	BB15	SMA_B6	SDQ_B2
MAAB_7	BA14	SMA_B7	SDQ_B3
MAAB_8	AY15	SMA_B8	SDQ_B4
MAAB_9	BB14	SMA_B9	SDQ_B5
MAAB_10	AW18	SMA_B10	SDQ_B6
MAAB_11	BB13	SMA_B11	SDQ_B7
MAAB_12	BA13	SMA_B12	
MAAB_13	AY29	SMA_B13	SDQS_B1
MAAB_14	AY13	SMA_B14	SDQS_B1#
			SDM_B1
SWE_L_B	BA27	SWE_B#	
SCAS_L_B	AW29	SCAS_B#	SDQ_B8
SRAS_L_B	AW26	SRAS_B#	SDQ_B9
			SDQ_B10
SBSB_0	AY19	SBS_B0	SDQ_B11
SBSB_1	BA18	SBS_B1	SDQ_B12
SBSB_2	BC12	SBS_B2	SDQ_B13
			SDQ_B14
CSB_L0	BB27	SCS_B0#	SDQ_B15
CSB_L1	BB30	SCS_B1#	
	AY27	RESERVED_13	SDQS_B2
	AY31	RESERVED_10	SDQS_B2#
			SDM_B2
CKEB_0	AY12	SCKE_B0	SDQ_B16
CKEB_1	AW12	SCKE_B1	SDQ_B17
	BB11	RESERVED_11	SDQ_B18
	BA11	RESERVED_12	SDQ_B19
ODTB_0	BA29	SODT_B0	SDQ_B20
ODTB_1	BA30	SODT_B1	SDQ_B21
	BB29	RESERVED_14	SDQ_B22
	BB31	RESERVED_15	SDQ_B23
DCLKB_H0	AV31	SCLK_B0	SDQS_B3
DCLKB_H1	AW32	SCLK_B0#	SDQS_B3#
DCLKB_L1	AT27	SCLK_B1	SDM_B3
DCLKB_H2	AV32	SCLK_B2	SDQ_B24
DCLKB_L2	AT32	SCLK_B2#	SDQ_B25
	AU29	RESERVED_16	SDQ_B26
	AR29	RESERVED_17	SDQ_B27
	AV29	RESERVED_18	SDQ_B28
	AW27	RESERVED_19	SDQ_B29
	AN33	RESERVED_20	SDQ_B30
	AP32	RESERVED_21	SDQ_B31
			SDQS_B4
			SDQS_B4#
			SDM_B4
			SDQ_B32
			SDQ_B33
			SDQ_B34
			SDQ_B35
			SDQ_B36
			SDQ_B37
			SDQ_B38
			SDQ_B39
SDQS_B5		AL35	DQS_H_B5
SDQS_B5#		AL34	DQS_L_B5
SDM_B5		AM37	MPD_B5
			SDQ_B40
			SDQ_B41
			SDQ_B42
			SDQ_B43
			SDQ_B44
			SDQ_B45
			SDQ_B46
			SDQ_B47
SDQS_B6		AG35	DQS_H_B6
SDQS_B6#		AG36	DQS_L_B6
SDM_B6		AG39	MPD_B6
			SDQ_B48
			SDQ_B49
			SDQ_B50
			SDQ_B51
			SDQ_B52
			SDQ_B53
			SDQ_B54
			SDQ_B55
SDQS_B7		AC36	DQS_H_B7
SDQS_B7#		AC37	DQS_L_B7
SDM_B7		AD38	MPD_B7
			SDQ_B56
			SDQ_B57
			SDQ_B58
			SDQ_B59
			SDQ_B60
			SDQ_B61
			SDQ_B62
			SDQ_B63

DDR_1

AM21

MCH VREF

SMRCOMP0

SMRCOMP1

SMRCOMP2

SMRCOMP3

SMRCOMP N

SMRCOMP P

SMRCOMPVOH

SMRCOMPVOH

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BC37	VSS_1	VSS_181	AF5
BC32	VSS_2	VSS_182	AF3
BC28	VSS_3	VSS_183	AF2
BC24	VSS_4	VSS_184	AF1
BC10	VSS_5	VSS_185	AD39
BC5	VSS_6	VSS_186	AD37
BB7	VSS_7	VSS_187	AD35
AY41	VSS_8	VSS_188	AD33
AY4	VSS_9	VSS_189	AD25
AW43	VSS_10	VSS_190	AD23
AW41	VSS_11	VSS_191	AD19
AW1	VSS_12	VSS_192	VSS_194
AV37	VSS_13	VSS_193	VSS_195
AV35	VSS_14	VSS_194	VSS_196
AV27	VSS_15	VSS_195	VSS_197
AV23	VSS_16	VSS_196	VSS_198
AV21	VSS_17	VSS_197	VSS_199
AV17	VSS_18	VSS_198	VSS_200
AV11	VSS_19	VSS_199	VSS_201
AV9	VSS_20	VSS_200	VSS_202
AV7	VSS_21	VSS_201	VSS_203
AU42	VSS_22	VSS_202	VSS_204
AU38	VSS_23	VSS_203	VSS_205
AU32	VSS_24	VSS_204	VSS_206
AU24	VSS_25	VSS_205	VSS_207
AU20	VSS_26	VSS_206	VSS_208
AU6	VSS_27	VSS_207	VSS_209
AU2	VSS_28	VSS_208	VSS_210
AT31	VSS_29	VSS_209	VSS_211
AT29	VSS_30	VSS_210	VSS_212
AT15	VSS_31	VSS_211	VSS_213
AT13	VSS_32	VSS_212	VSS_214
AT12	VSS_33	VSS_213	VSS_215
AR38	VSS_34	VSS_214	VSS_216
AR33	VSS_35	VSS_215	VSS_217
AR32	VSS_36	VSS_216	VSS_218
AR27	VSS_37	VSS_217	VSS_219
AR26	VSS_38	VSS_218	VSS_220
AR23	VSS_39	VSS_219	VSS_221
AR21	VSS_40	VSS_220	VSS_222
AR20	VSS_41	VSS_221	VSS_223
AR17	VSS_42	VSS_222	VSS_224
AR9	VSS_43	VSS_223	VSS_225
AR6	VSS_44	VSS_224	VSS_226
AP43	VSS_45	VSS_225	VSS_227
AP24	VSS_46	VSS_226	VSS_228
AP18	VSS_47	VSS_227	VSS_229
AP1	VSS_48	VSS_228	VSS_230
AN38	VSS_49	VSS_229	VSS_231
AN31	VSS_50	VSS_230	VSS_232
AN29	VSS_51	VSS_231	VSS_233
AN24	VSS_52	VSS_232	VSS_234
AN23	VSS_53	VSS_233	VSS_235
AN20	VSS_54	VSS_234	VSS_236
AN15	VSS_55	VSS_235	VSS_237
AN13	VSS_56	VSS_236	VSS_238
AN12	VSS_57	VSS_237	VSS_239
AN11	VSS_58	VSS_238	VSS_240
AN4	VSS_59	VSS_239	VSS_241
AM42	VSS_60	VSS_240	VSS_242
AM40	VSS_61	VSS_241	VSS_243
AM36	VSS_62	VSS_242	VSS_244
AM33	VSS_63	VSS_243	VSS_245
AM29	VSS_64	VSS_244	VSS_246
AM24	VSS_65	VSS_245	VSS_247
AM23	VSS_66	VSS_246	VSS_248
AM20	VSS_67	VSS_247	VSS_249
AM11	VSS_68	VSS_248	VSS_250
AM9	VSS_69	VSS_249	
AM7	VSS_70	VSS_250	

GND

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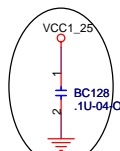
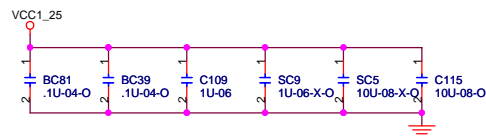
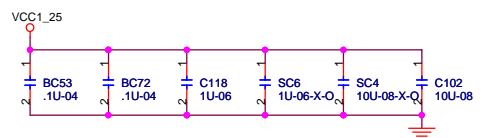
LE82G31-80

AM4	VSS_71	VSS_250	R5
AM2	VSS_72	VSS_251	R3
AM1	VSS_73	VSS_252	P43
AL36	VSS_74	VSS_253	P30
AL33	VSS_75	VSS_254	P21
AK43	VSS_76	VSS_255	P18
AJ39	VSS_77	VSS_256	P17
AJ36	VSS_78	VSS_257	P2
AJ33	VSS_79	VSS_258	N36
AH42	VSS_80	VSS_259	N33
AG37	VSS_81	VSS_260	N31
AG34	VSS_82	VSS_261	N27
AF43	VSS_83	VSS_262	N21
AF37	VSS_84	VSS_263	N13
AF36	VSS_85	VSS_264	N10
AF10	VSS_86	VSS_265	N7
AF9	VSS_87	VSS_266	N5
AF8	VSS_88	VSS_267	M42
AF7	VSS_89	VSS_268	M37
AF6	VSS_90	VSS_269	M35
AC5	VSS_91	VSS_270	M33
AB43	VSS_92	VSS_271	BC41
AB25	VSS_93	VSS_272	BC3
AB23	VSS_94	VSS_273	BA1
AB21	VSS_95	VSS_274	AY40
AB19	VSS_96	VSS_275	AF23
AB2	VSS_97	VSS_276	AF21
AB1	VSS_98	VSS_277	AF19
AA38	VSS_99	VSS_278	AE24
AA35	VSS_100	VSS_279	AE22
AA24	VSS_101	VSS_280	AE20
AA22	VSS_102	VSS_281	AE18
AA20	VSS_103	VSS_282	AC18
AA8	VSS_104	VSS_283	AA18
AA5	VSS_105	VSS_284	W24
Y42	VSS_106	VSS_285	W22
Y37	VSS_107	VSS_286	W20
Y35	VSS_108	VSS_287	E1
Y33	VSS_109	VSS_288	E1
Y25	VSS_110	VSS_289	C43
Y23	VSS_111	VSS_290	C1
Y21	VSS_112	VSS_291	A41
Y19	VSS_113	VSS_292	A5
Y10	VSS_114	VSS_293	A3
Y7	VSS_115		
Y5	VSS_116		
Y1	VSS_117		
W3	VSS_118		
W3	VSS_119		
W3	VSS_120		
W3	VSS_121		
W3	VSS_122		
W3	VSS_123		
W3	VSS_124		
W3	VSS_125		
W3	VSS_126		
W3	VSS_127		
W3	VSS_128		
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W3	VSS_153		
W3	VSS_154		
W3	VSS_155		
W3	VSS_156		
W3	VSS_157		
W3	VSS_158		

GND

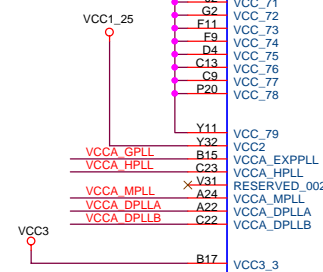
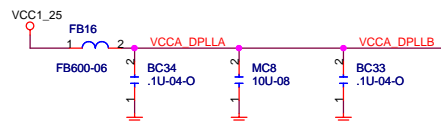
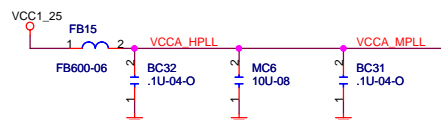
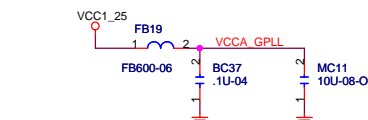
7 OF 7

LE82G31-80



正面

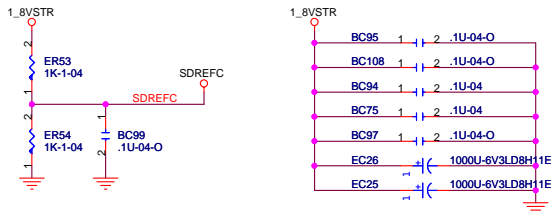
正面



BC37	VSS_1	VSS_181	AF5
BC32	VSS_2	VSS_182	AF3
BC28	VSS_3	VSS_183	AF2
BC24	VSS_4	VSS_184	AF1
BC10	VSS_5	VSS_185	AD39
BC5	VSS_6	VSS_186	AD37
BB7	VSS_7	VSS_187	AD35
AY41	VSS_8	VSS_188	AD33
AY4	VSS_9	VSS_189	AD25
AW43	VSS_10	VSS_190	AD23
AW41	VSS_11	VSS_191	AD19
AW1	VSS_12	VSS_192	VSS_194
AV37	VSS_13	VSS_193	VSS_195
AV35	VSS_14	VSS_194	VSS_196
AV27	VSS_15	VSS_195	VSS_197
AV23	VSS_16	VSS_196	VSS_198
AV21	VSS_17	VSS_197	VSS_199
AV17	VSS_18	VSS_198	VSS_200
AV11	VSS_19	VSS_199	VSS_201
AV9	VSS_20	VSS_200	VSS_202
AV7	VSS_21	VSS_201	VSS_203
AU42	VSS_22	VSS_202	VSS_204
AU38	VSS_23	VSS_203	VSS_205
AU32	VSS_24	VSS_204	VSS_206
AU24	VSS_25	VSS_205	VSS_207
AU20	VSS_26	VSS_206	VSS_208
AU6	VSS_27	VSS_207	VSS_209
AU2	VSS_28	VSS_208	VSS_210
AT31	VSS_29	VSS_209	VSS_211
AT29	VSS_30	VSS_210	VSS_212
AT15	VSS_31	VSS_211	VSS_213
AT13	VSS_32	VSS_212	VSS_214
AT12	VSS_33	VSS_213	VSS_215
AR38	VSS_34	VSS_214	VSS_216
AR33	VSS_35	VSS_215	VSS_217
AR32	VSS_36	VSS_216	VSS_218
AR27	VSS_37	VSS_217	VSS_219
AR26	VSS_38	VSS_218	VSS_220
AR23	VSS_39	VSS_219	VSS_221
AR21	VSS_40	VSS_220	VSS_222
AR20	VSS_41	VSS_221	VSS_223
AR17	VSS_42	VSS_222	VSS_224
AR9	VSS_43	VSS_223	VSS_225
AR6	VSS_44	VSS_224	VSS_226
AP43	VSS_45	VSS_225	VSS_227
AP24	VSS_46	VSS_226	VSS_228
AP18	VSS_47	VSS_227	VSS_229
AP1	VSS_48	VSS_228	VSS_230
AN38	VSS_49	VSS_229	VSS_231
AN31	VSS_50	VSS_230	VSS_232
AN29	VSS_51	VSS_231	VSS_233
AN24	VSS_52	VSS_232	VSS_234
AN23	VSS_53	VSS_233	VSS_235
AN20	VSS_54	VSS_234	VSS_236
AN15	VSS_55	VSS_235	VSS_237
AN13	VSS_56	VSS_236	VSS_238
AN12	VSS_57	VSS_237	VSS_239
AN11	VSS_58	VSS_238	VSS_240
AN4	VSS_59	VSS_239	VSS_241
AM42	VSS_60	VSS_240	VSS_242
AM40	VSS_61	VSS_241	VSS_243
AM36	VSS_62	VSS_242	VSS_244
AM33	VSS_63	VSS_243	VSS_245
AM29	VSS_64	VSS_244	VSS_246
AM24	VSS_65	VSS_245	VSS_247
AM23	VSS_66	VSS_246	VSS_248
AM20	VSS_67	VSS_247	VSS_249
AM11	VSS_68	VSS_248	VSS_250
AM9	VSS_69	VSS_249	
AM7	VSS_70	VSS_250	

POWER

LE82G31-80



14 DCLKB_H[0..2] << DCLKB_H[0..2]

14 ODTB_0[0..1] << ODTB_0[0..1]

14 SSB_S_0[0..2] << SSB_S_0[0..2]

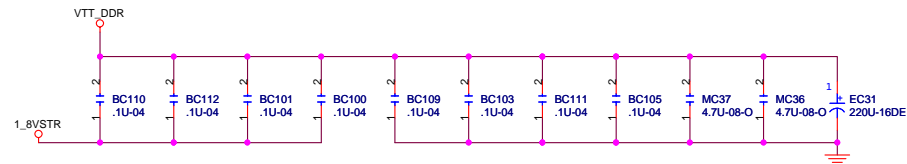
14 SWE_L_B << SWE_L_B

14 SCAS_L_B << SCAS_L_B

14 SRAS_L_B << SRAS_L_B

8,17,19,21,23 SMBDATA << SMBDATA

8,17,19,21,23 SMBCLK << SMBCLK



14 MD_B[0..63] << MD_B[0..63]

14 DQS_L_B[0..7] << DQS_L_B[0..7]

14 DQS_H_B[0..7] << DQS_H_B[0..7]

14 MPD_B[0..7] << MPD_B[0..7]

14 MAAB_0[0..14] << MAAB_0[0..14]

14 CSB_L[0..1] << CSB_L[0..1]

14 CKEB_0[0..1] << CKEB_0[0..1]

14 DCLKB_L[0..2] << DCLKB_L[0..2]

14 DCLKA_L[0..2] << DCLKA_L[0..2]

14 DCLKA_H[0..2] << DCLKA_H[0..2]

14 ODTA_0[0..1] << ODTA_0[0..1]

14 SBSA_0[0..2] << SBSA_0[0..2]

14 SWE_L_A << SWE_L_A

14 SCAS_L_A << SCAS_L_A

14 SRAS_L_A << SRAS_L_A

14 MD_A[0..63] << MD_A[0..63]

14 DQS_L_A[0..7] << DQS_L_A[0..7]

14 DQS_H_A[0..7] << DQS_H_A[0..7]

14 MPD_A[0..7] << MPD_A[0..7]

14 MAAA_0[0..14] << MAAA_0[0..14]

14 CSA_L[0..1] << CSA_L[0..1]

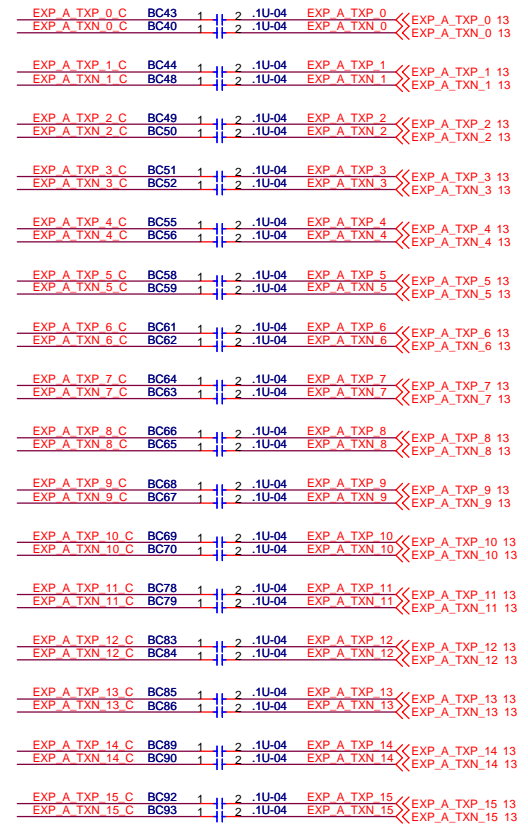
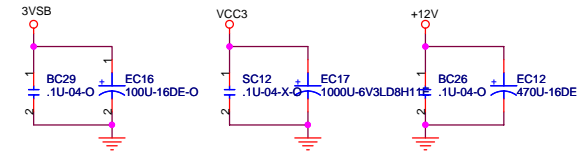
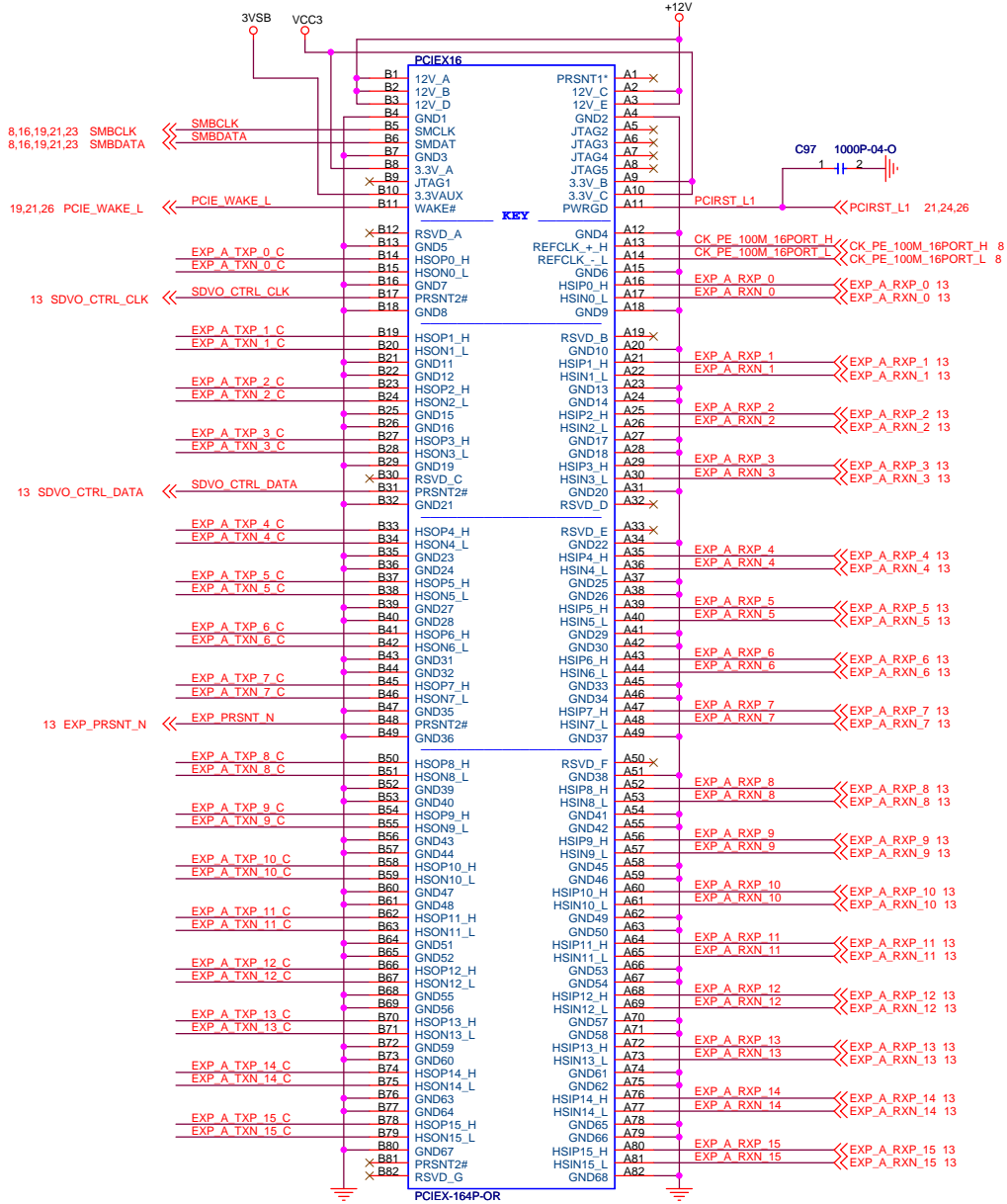
14 CKEA_0[0..1] << CKEA_0[0..1]

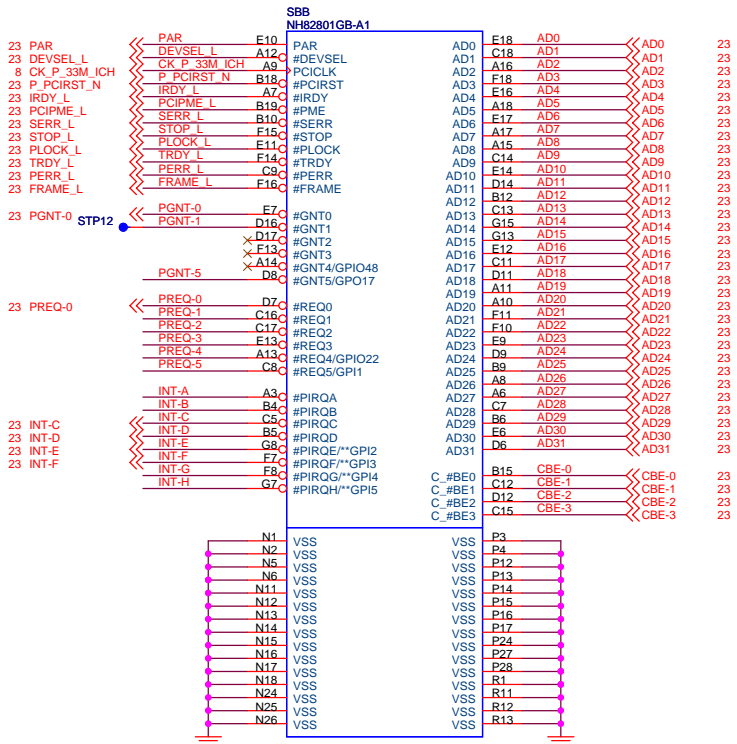
Elitegroup Computer Systems

File **DDIMM 1&2 (DDR SDRAMs)**

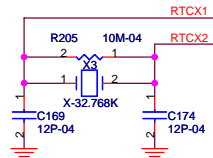
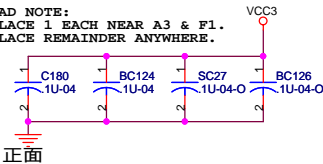
Size Document Number **G31T-M9** Rev 7.0

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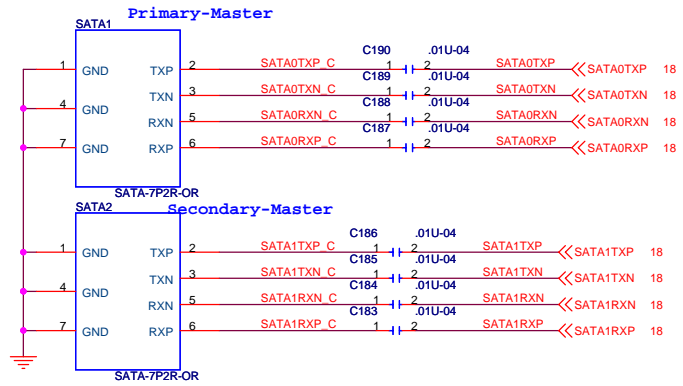
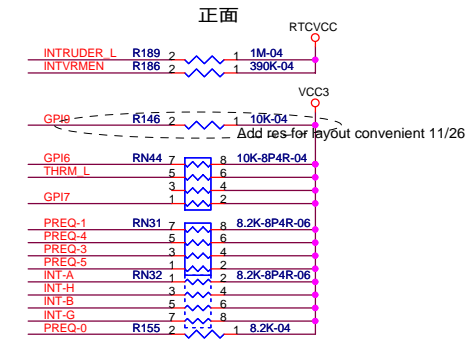
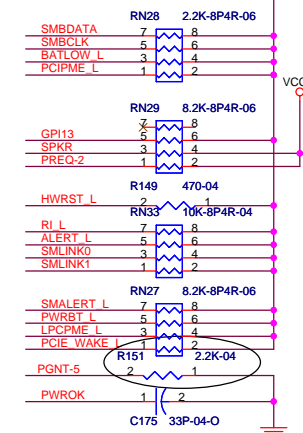
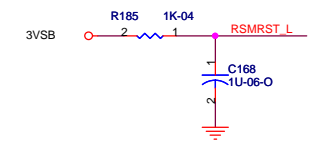
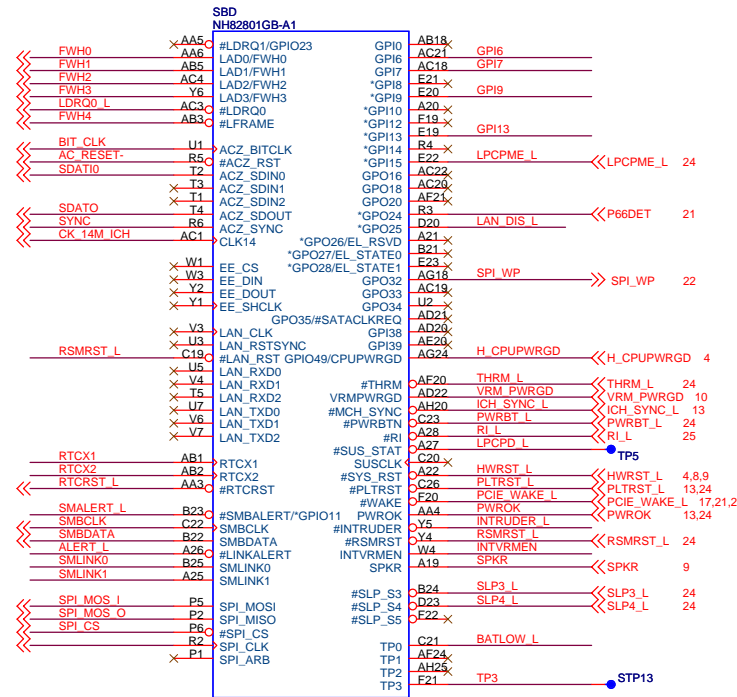


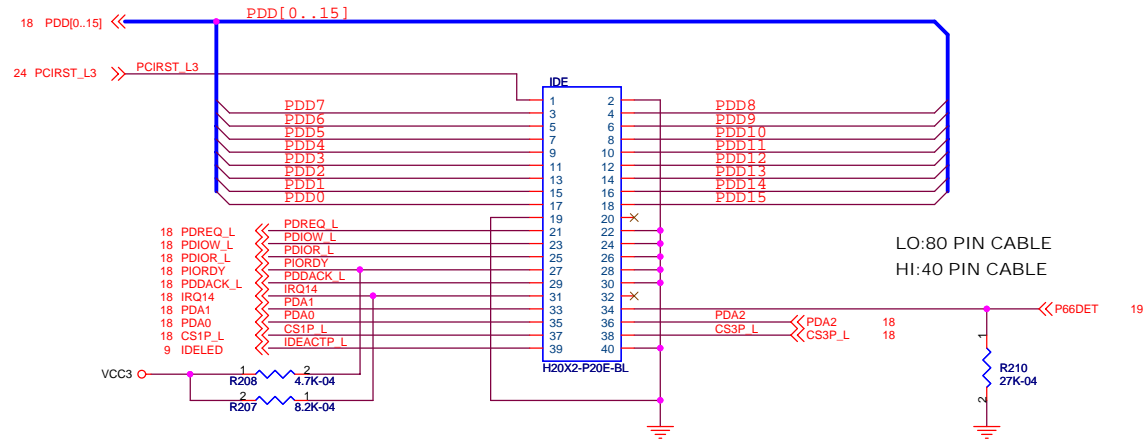


CAD NOTE:
PLACE 1 EACH NEAR A3 & F1.
PLACE REMAINDER ANYWHERE.

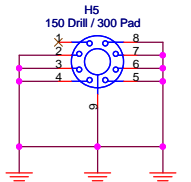
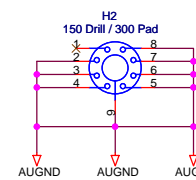
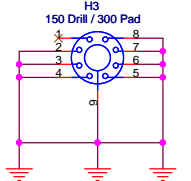
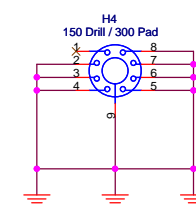
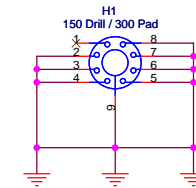
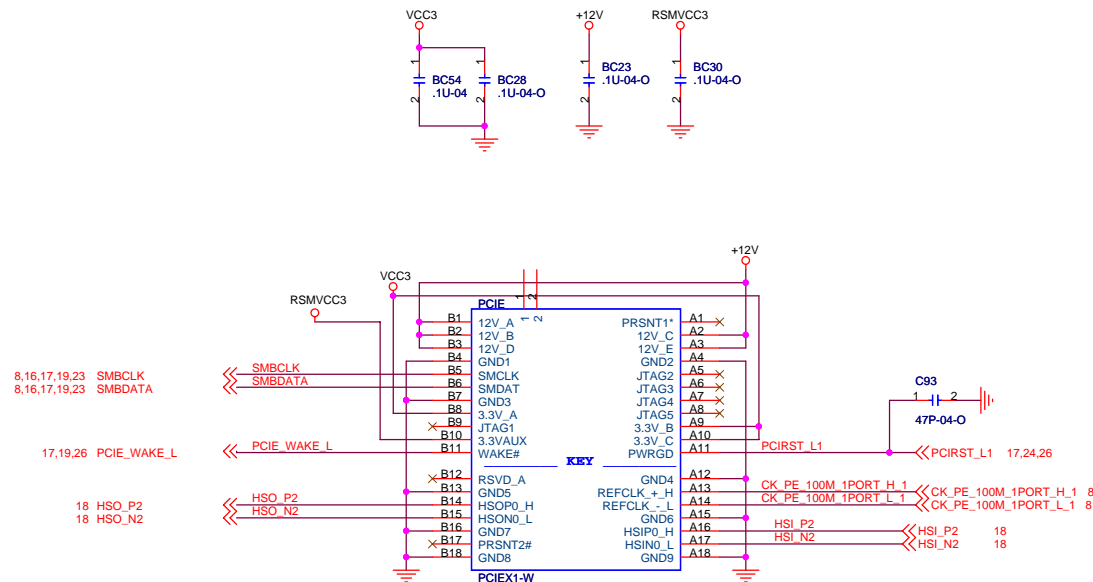


For 103
X3(wire)
JP-W1-P6.25

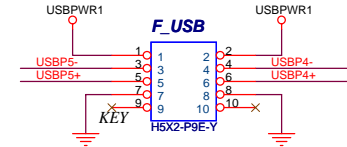
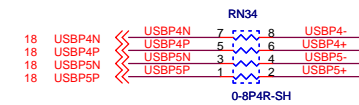
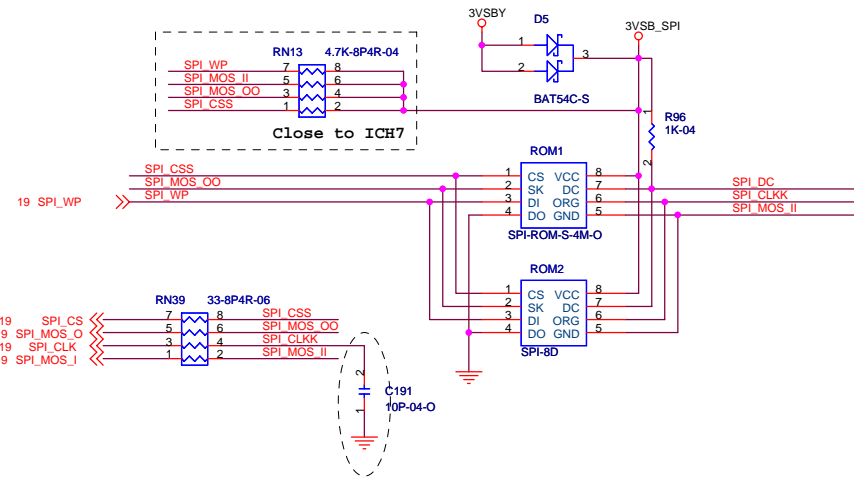
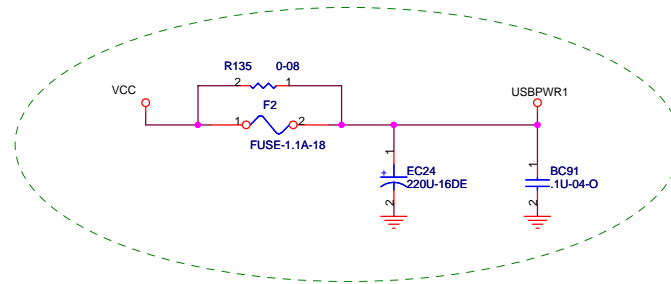
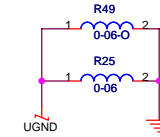
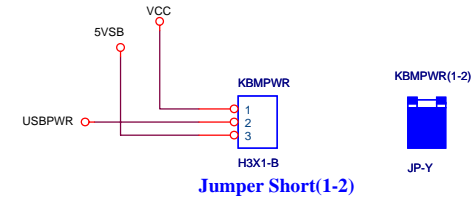
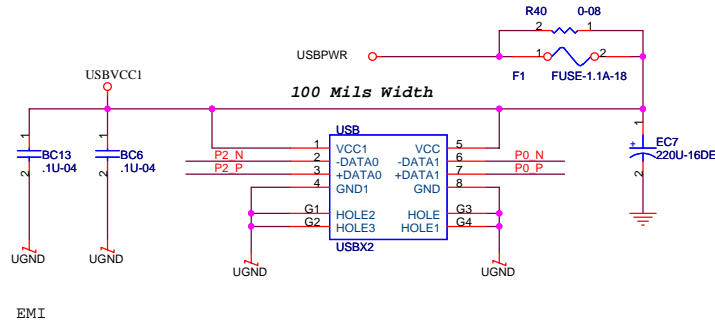
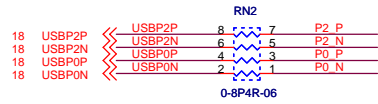




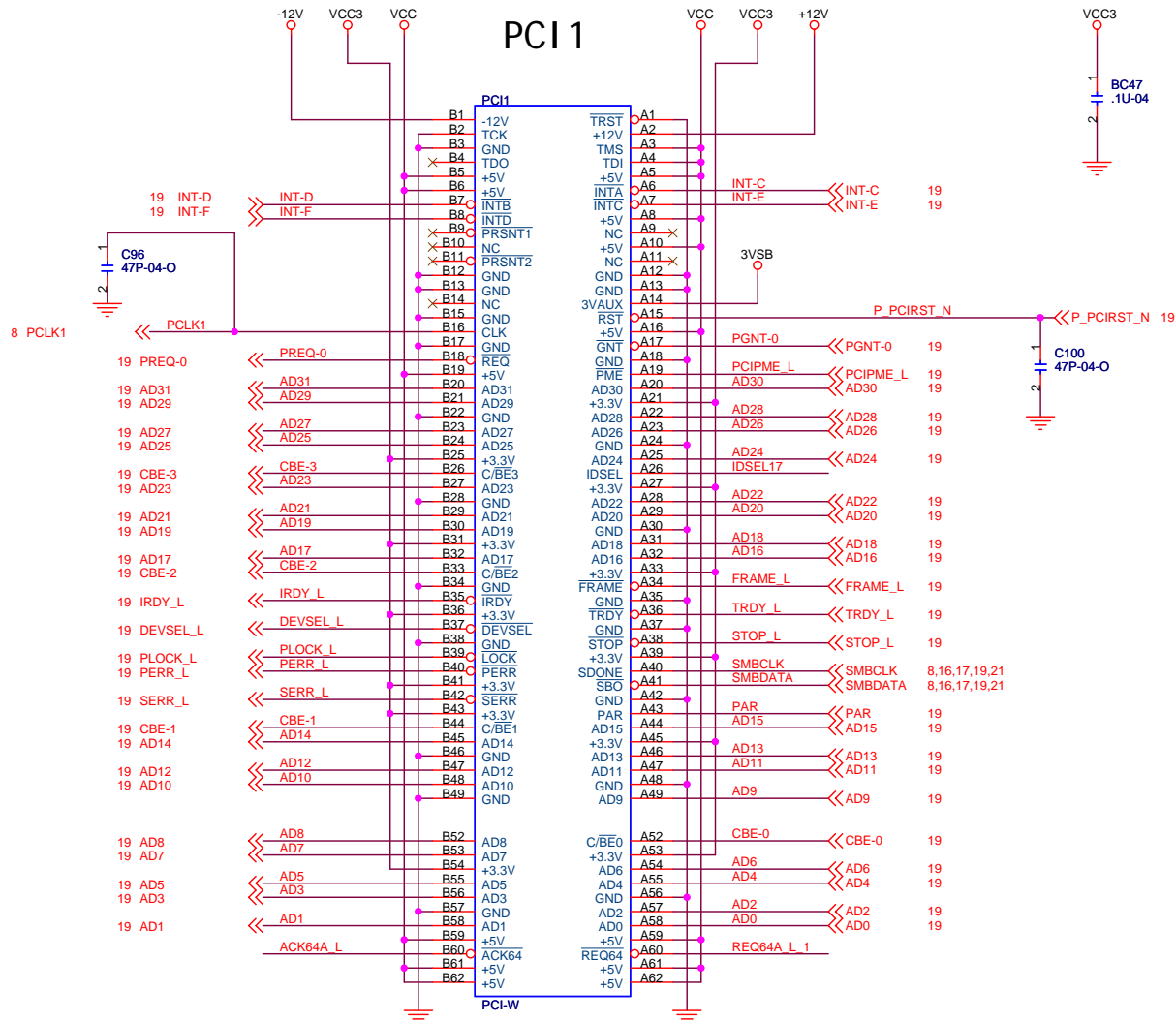
DATA LINES SHOULD BE MATCHED TO STROBES (PDIOR_L , PIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.



REAR_SIDE

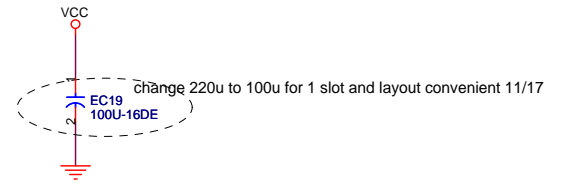
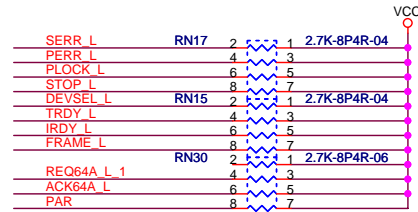


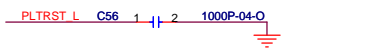
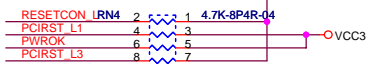
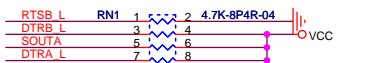
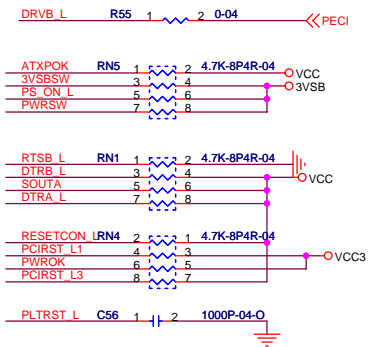
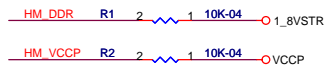
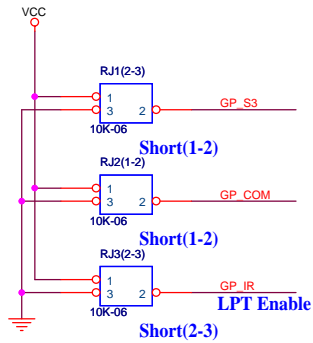
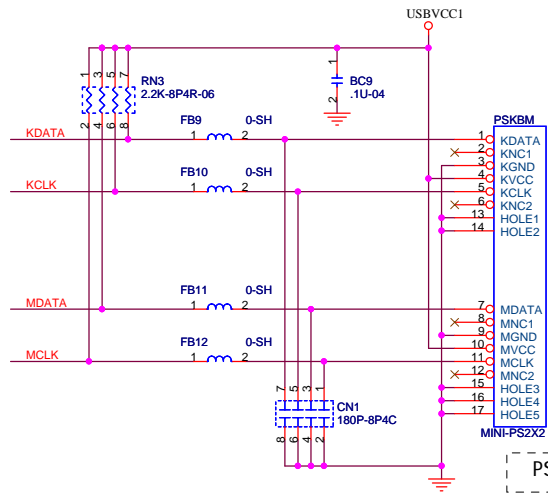
PCI 1



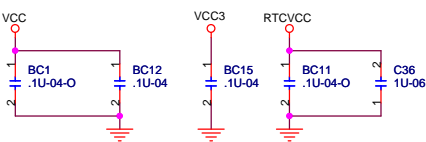
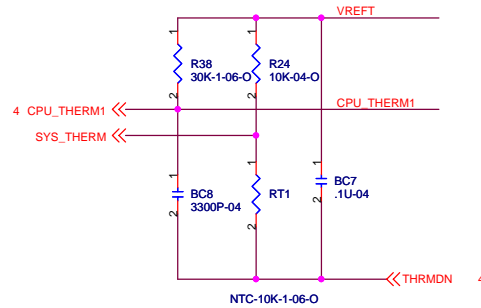
PCI1-INT: IDSEL=AD17
 INTA:INTC REQ=PREQ0#
 INTB:INTD GNT=PGNT0#
 INTC:INTE
 INTD:INTF

R94 300-04 AD17 IDSEL17

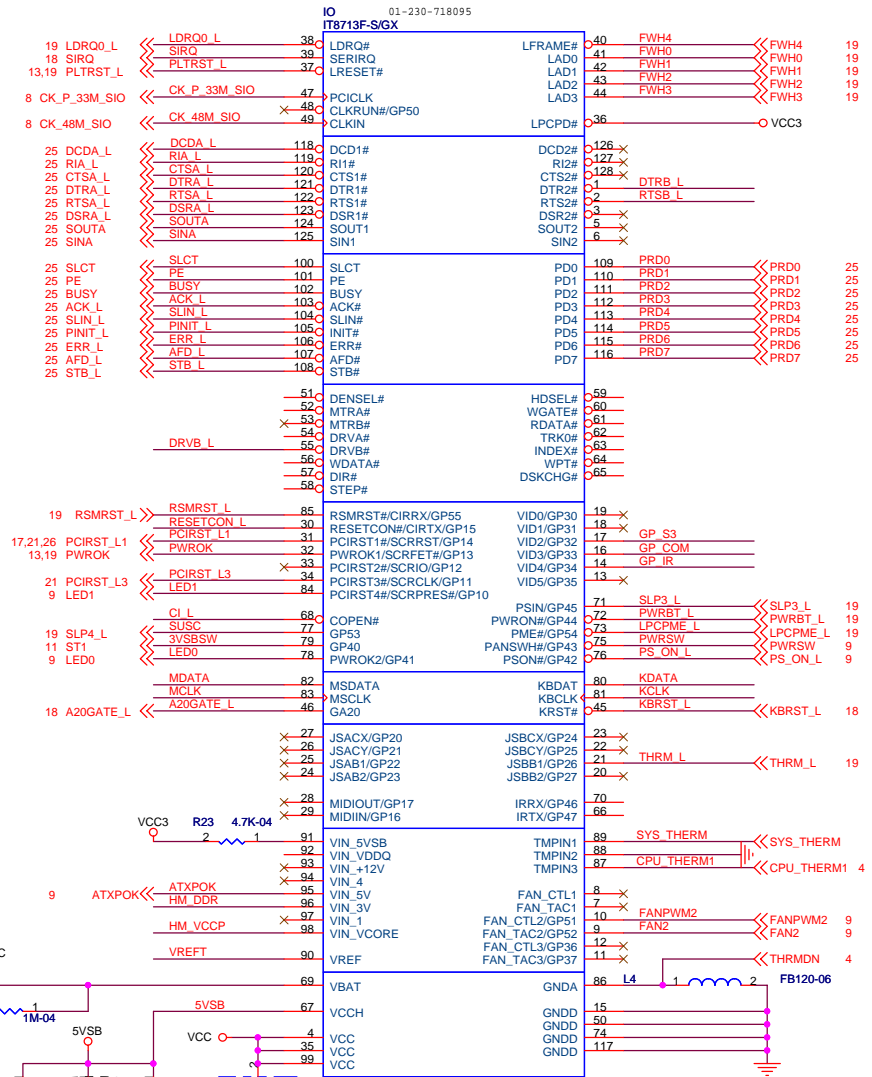




THERM. SENSING



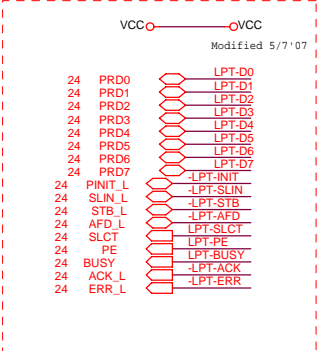
修改U3 Value:8718F



MC47 close IO Pin for EC126 Placement inconvenient 1117

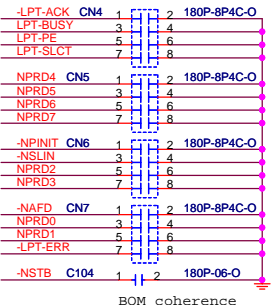
LPT

External Connection

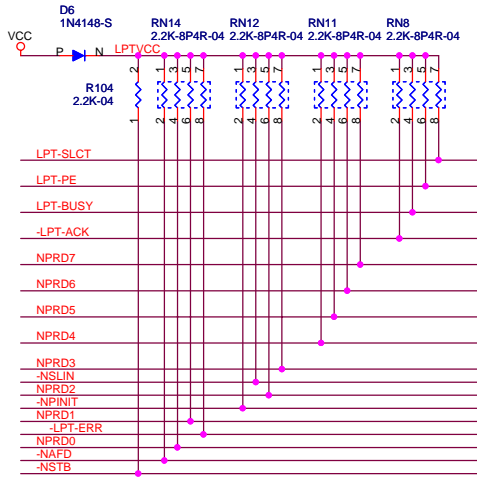


If you found anything wrong with this circuit, please contact with Jack Hu (Ext:622)

LPT-D4	NPRD4
LPT-D5	NPRD5
LPT-D6	NPRD6
LPT-D7	NPRD7
-LPT-INIT	-NPINIT
-LPT-SLIN	-NSLIN
LPT-D2	NPRD2
LPT-D3	NPRD3
-LPT-STB	-NSTB
-LPT-AFD	-NAFD
LPT-D0	NPRD0
LPT-D1	NPRD1



BOM coherence

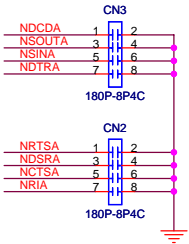
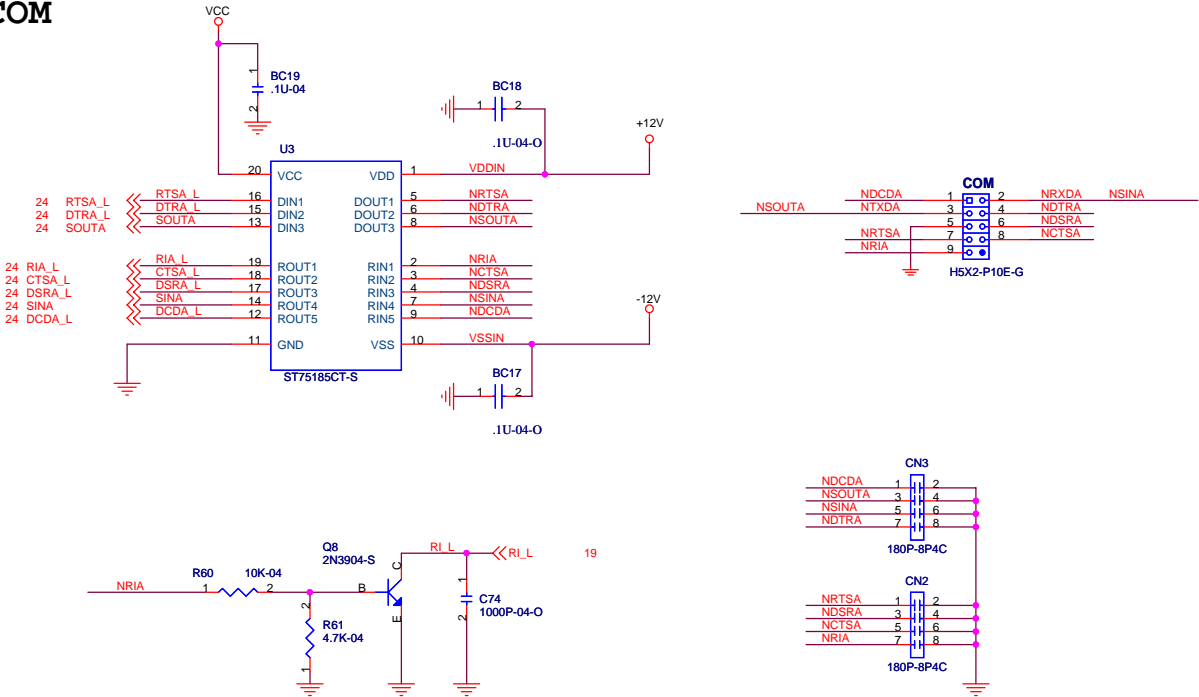


Selection design with LPT1

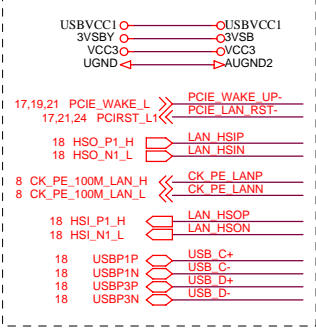
LPT			
-NSTB	1	STB	14
NPRD0	2	PD0	15
NPRD1	3	PD1	16
NPRD2	4	PD2	17
NPRD3	5	PD3	18
NPRD4	6	PD4	19
NPRD5	7	PD5	20
NPRD6	8	PD6	21
NPRD7	9	PD7	22
-LPT-ACK	10	ACK	23
LPT-BUSY	11	BUSY	24
LPT-PE	12	PE	25
LPT-SLCT	13	SLCT	

H13X2-P26E-B

COM



External Connection



When you found some bug, please inform Ren(ext:665) to update circuit.

RTL8103EL-GR
01-278-103350

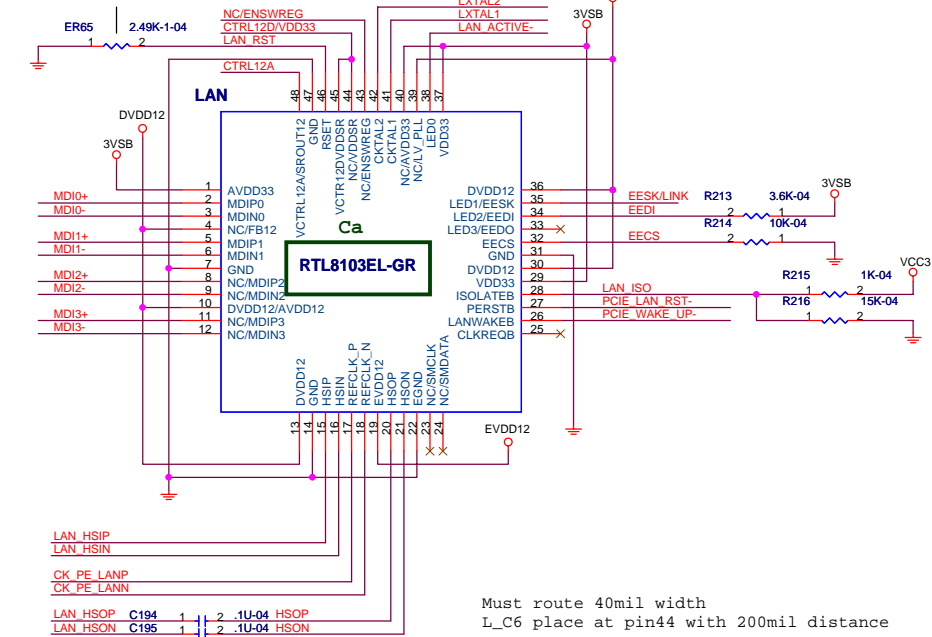
BOM Difference

	RTL8111DL-GR 1000M	RTL8103EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8103EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100

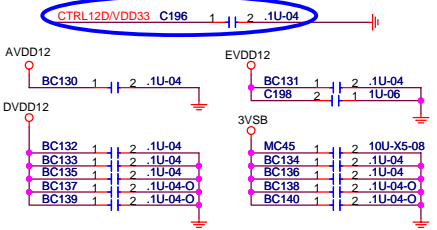
Power Difference

	RTL8111D	RTL8103E
AVDD33 VDD33	3.3V 3VSB供應	3.3V 3VSB供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應

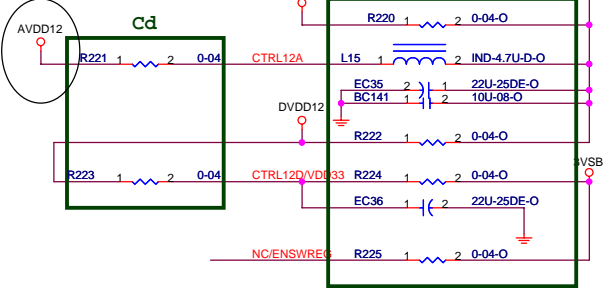
RSET電阻需close to LAN
Trace need GND shielding



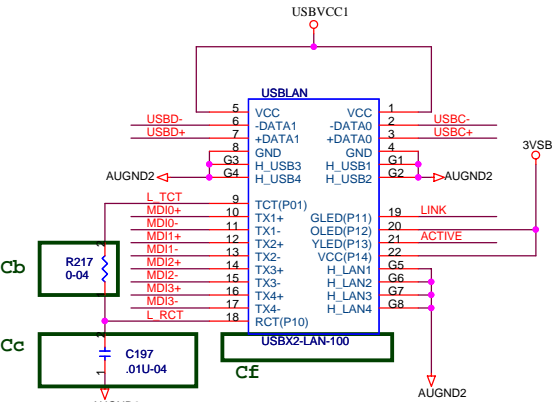
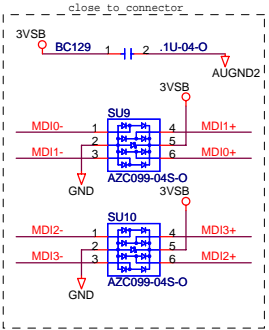
Must route 40mil width
L_C6 place at pin44 with 200mil distance



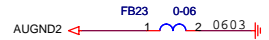
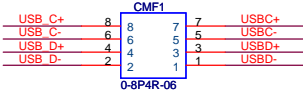
L_L1 & L_R9 place at pin48 with 200mil distance
L_EC1 place at near L_L1
Must route 60mil width



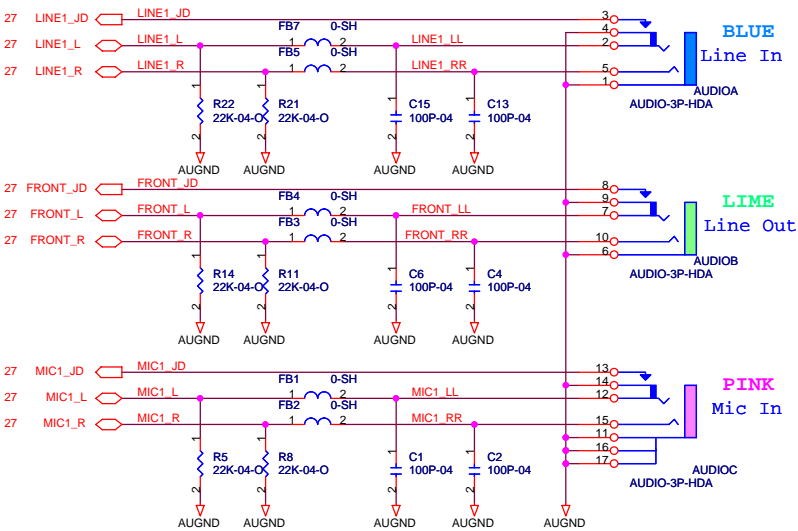
Choke near pin48,
E/C cap near Choke



Link: Green on
Active: Yellow blinking



REAR-AUDIO



FRONT-AUDIO

